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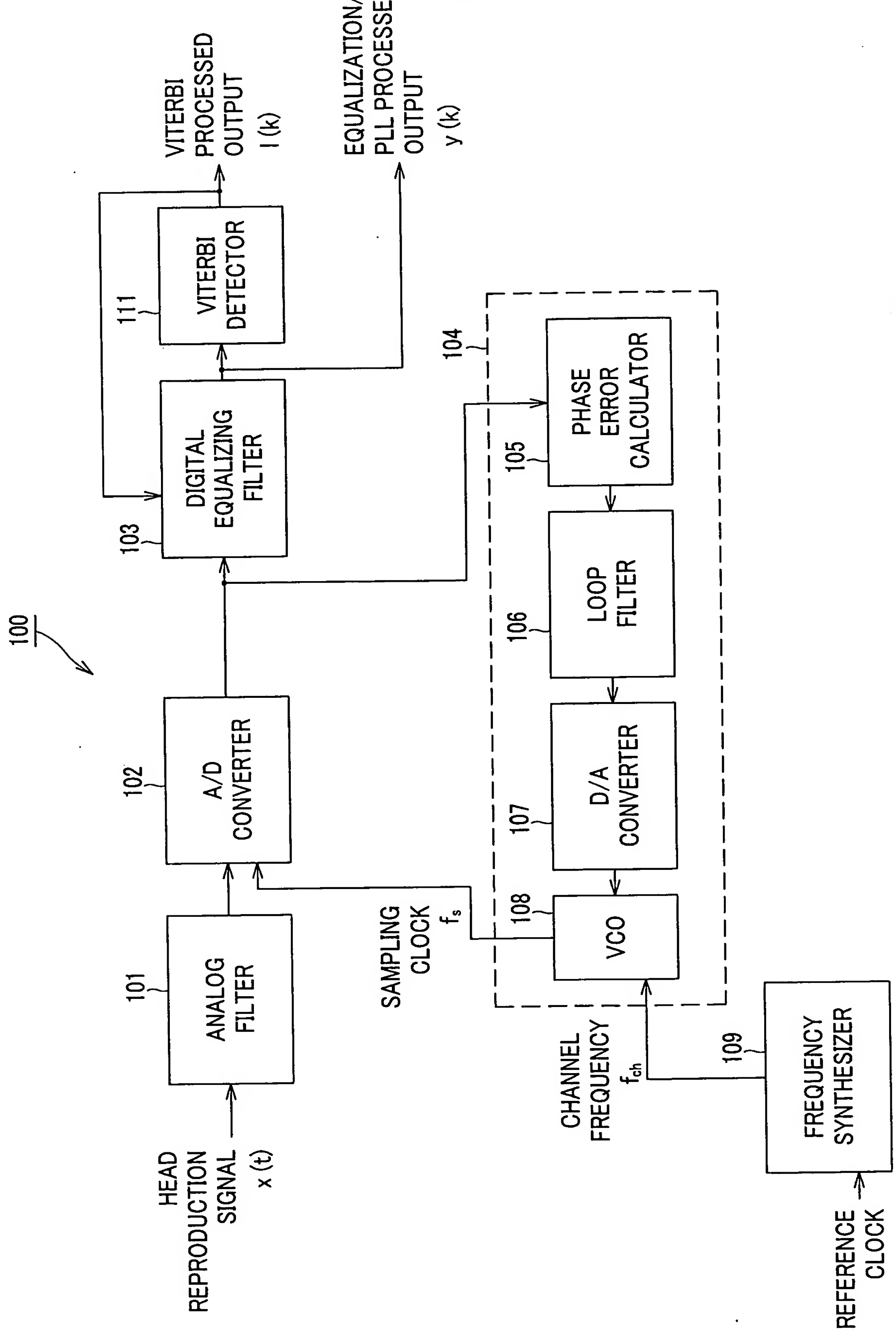

FIG.1

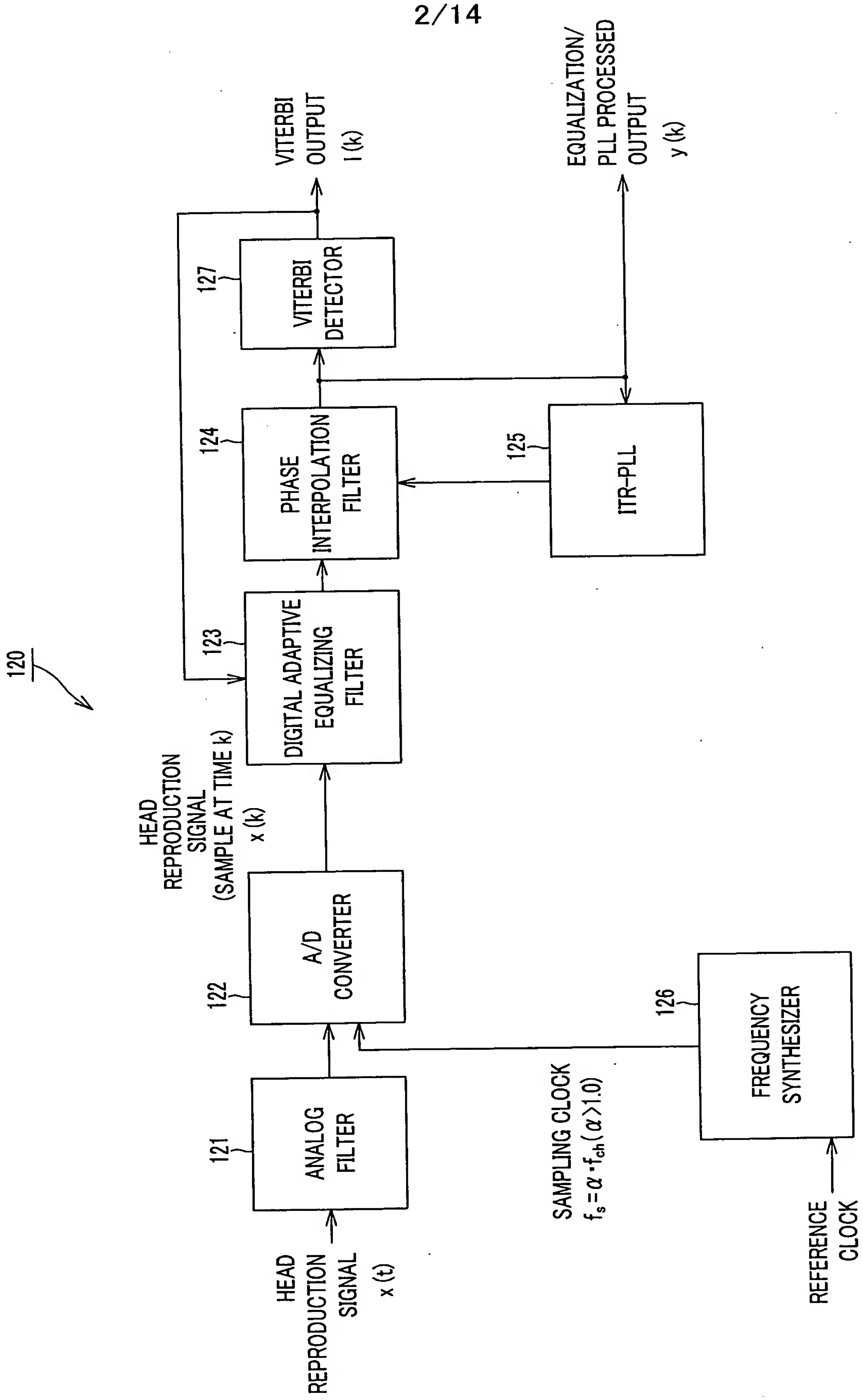
120
HEAD REPRODUCTION SIGNAL x (t)
121
ANALOG FILTER
122
A/D CONVERTER
HEAD REPRODUCTION SIGNAL (SAMPLE AT TIME k) x (k)
123
DIGITAL ADAPTIVE EQUALIZING FILTER
124
PHASE INTERPOLATION FILTER
125
ITR-PLL
127
VITERBI DETECTOR
VITERBI OUTPUT I (k)
EQUALIZATION/ PLL PROCESSED OUTPUT y (k)
SAMPLING CLOCK $f_s=\alpha\cdot f_{ch}(\alpha>1.0)$
126
FREQUENCY SYNTHESIZER
REFERENCE CLOCK

FIG.2

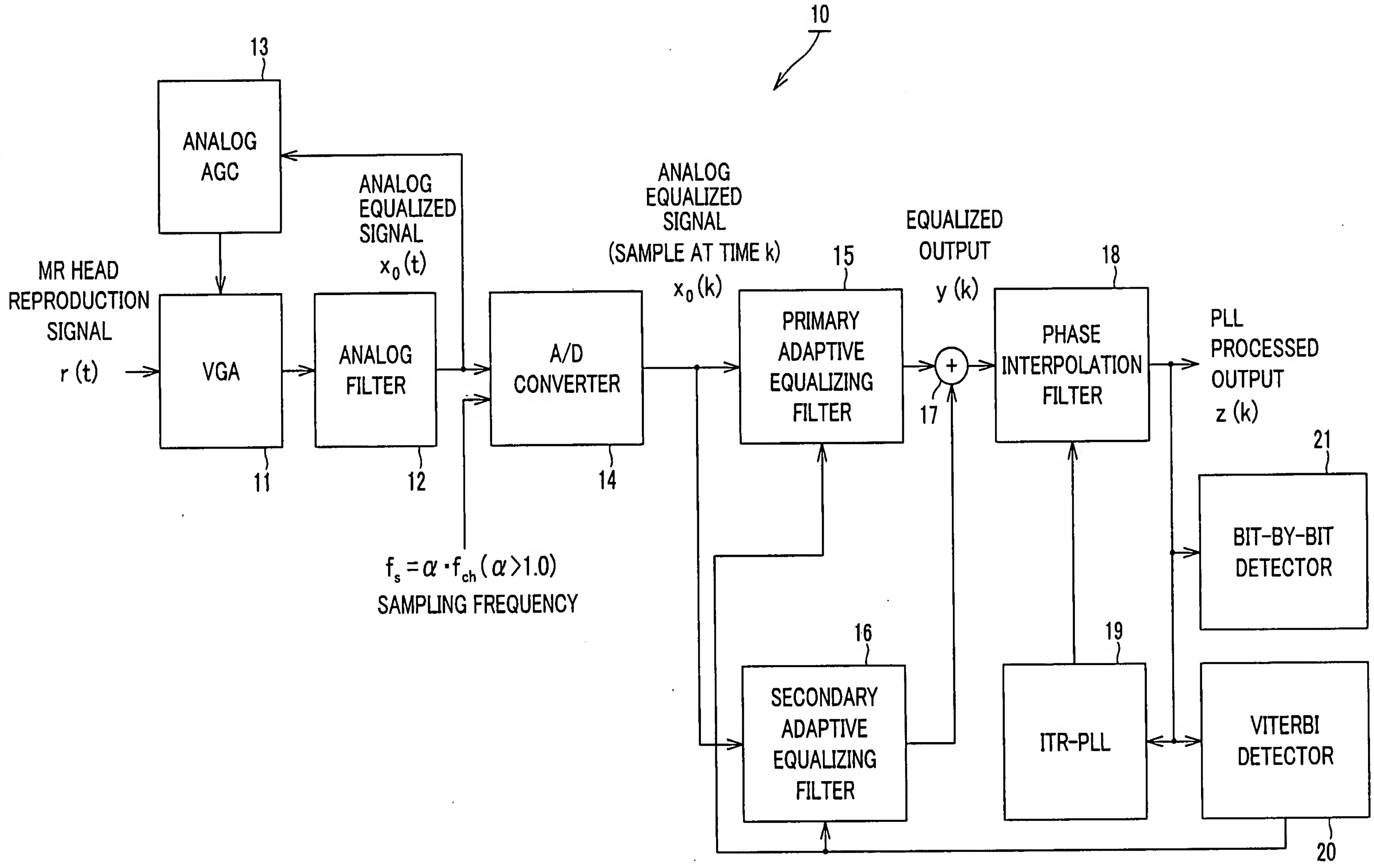
10
13
ANALOG AGC
MR HEAD REPRODUCTION SIGNAL
r (t)
VGA
11
ANALOG FILTER
12
ANALOG EQUALIZED SIGNAL
$x_0(t)$
A/D CONVERTER
14
$f_s=\alpha\cdot f_{ch}(\alpha>1.0)$
SAMPLING FREQUENCY
ANALOG EQUALIZED SIGNAL
(SAMPLE AT TIME k)
$x_0(k)$
15
PRIMARY ADAPTIVE EQUALIZING FILTER
16
SECONDARY ADAPTIVE EQUALIZING FILTER
EQUALIZED OUTPUT
y (k)
17
+
18
PHASE INTERPOLATION FILTER
19
ITR-PLL
PLL PROCESSED OUTPUT
z (k)
21
BIT-BY-BIT DETECTOR
VITERBI DETECTOR
20

FIG.3

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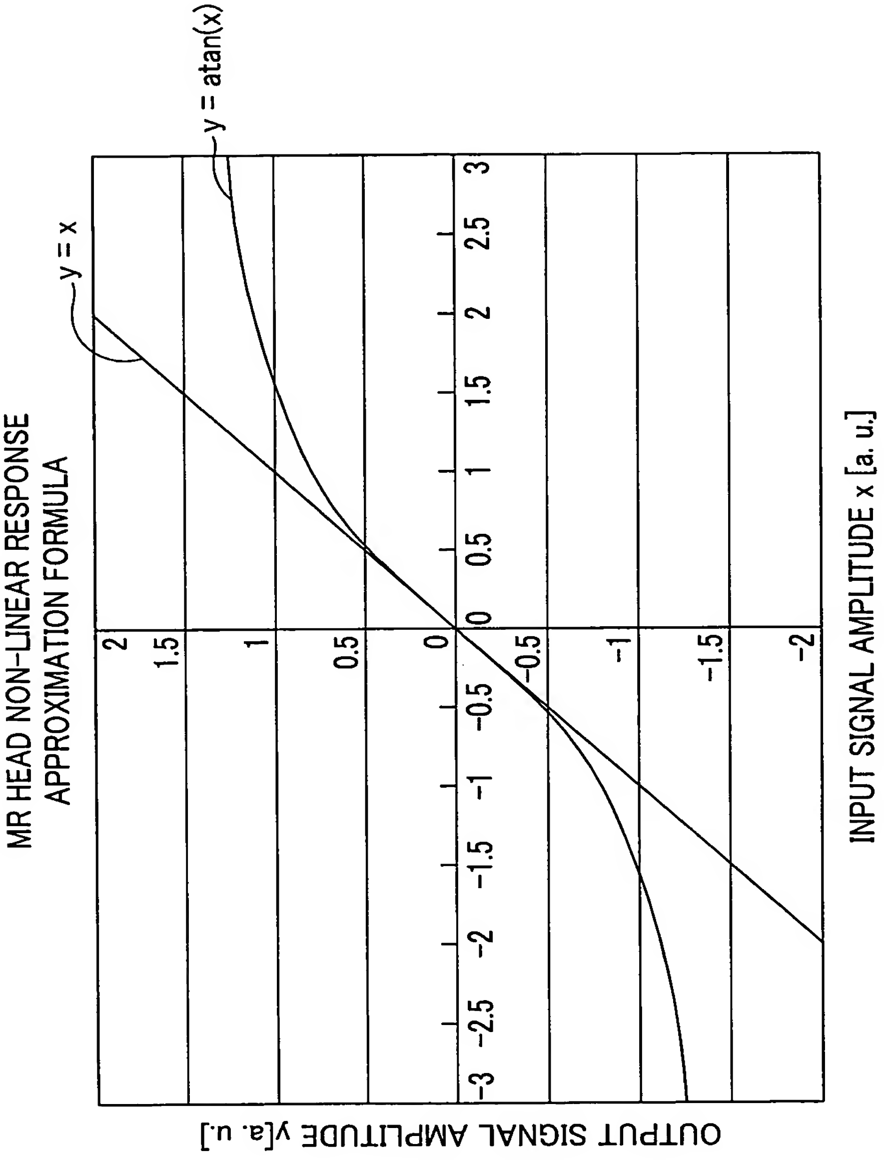

FIG.4

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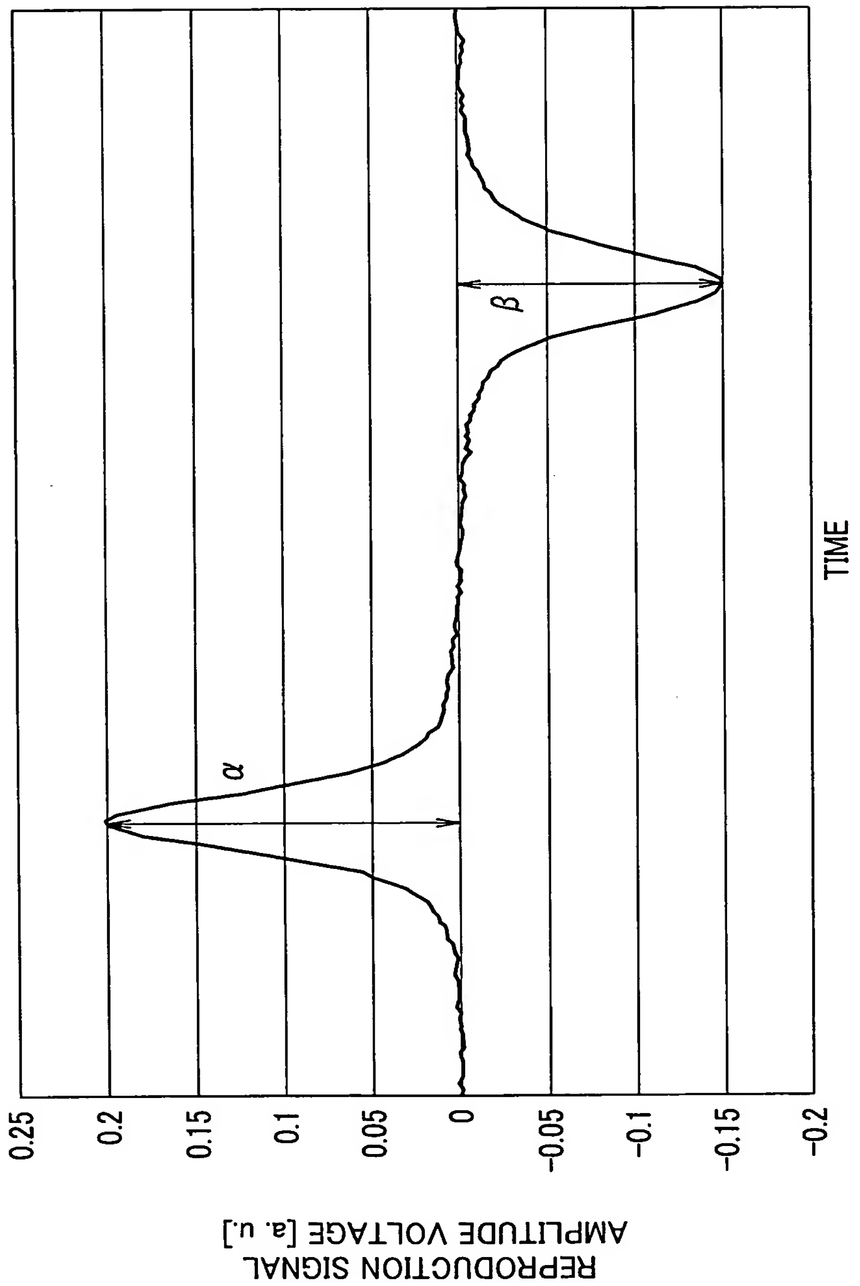

FIG.5

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	Δx = 0.0	Δx = 0.2	Δx = 0.4	Δx = 0.6	Δx = 0.8	Δx = 0.10
R	0	0.083708	0.153591	0.202075	0.229168	0.239529

FIG.6

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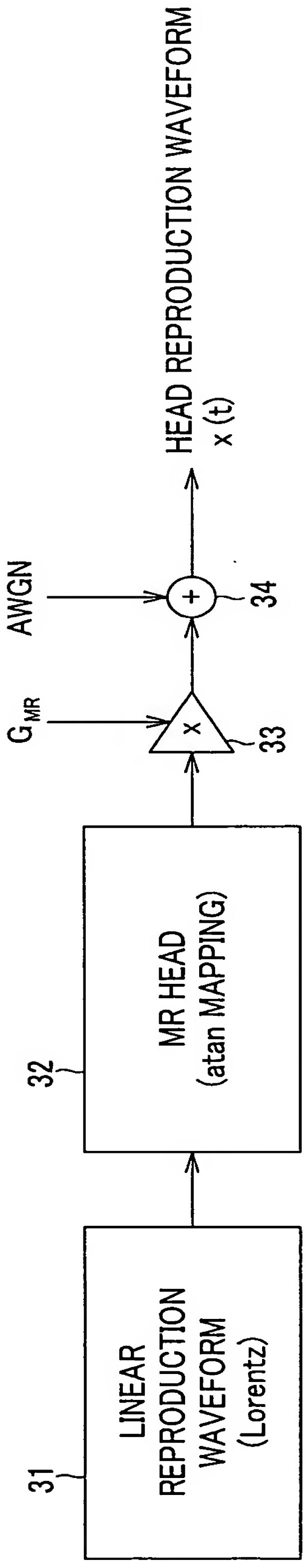

FIG.7

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S04P0693

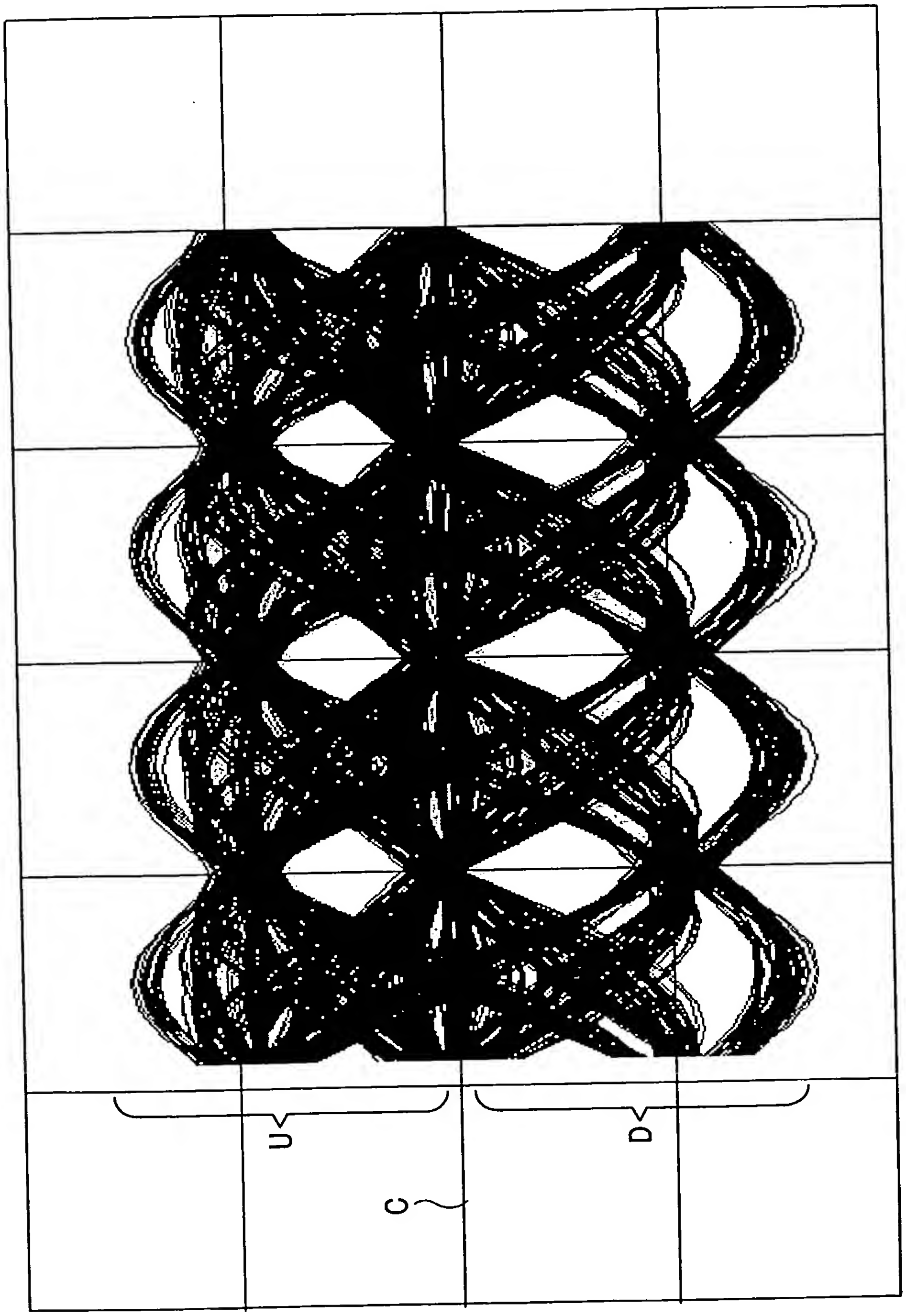

FIG.8

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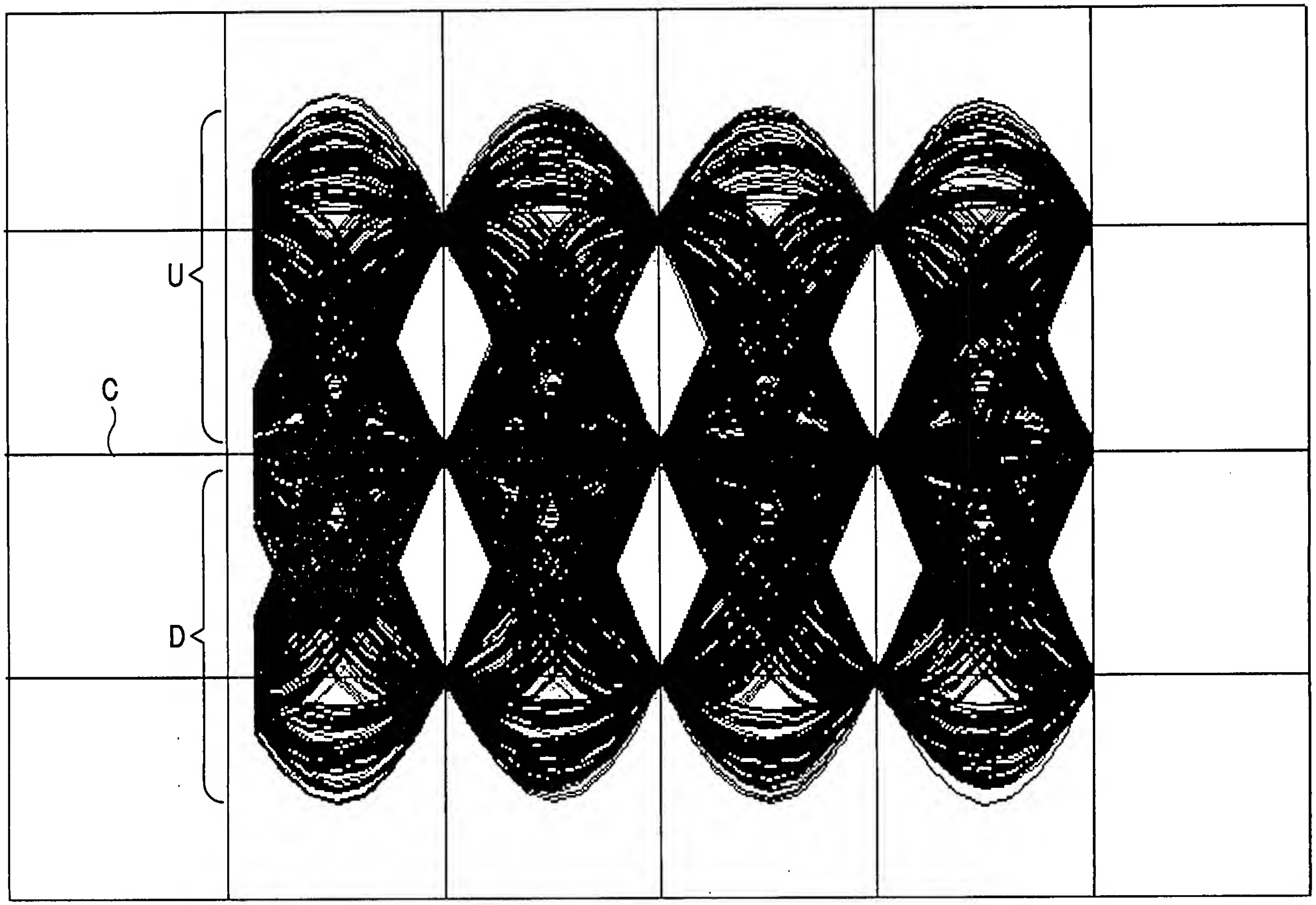

FIG.9

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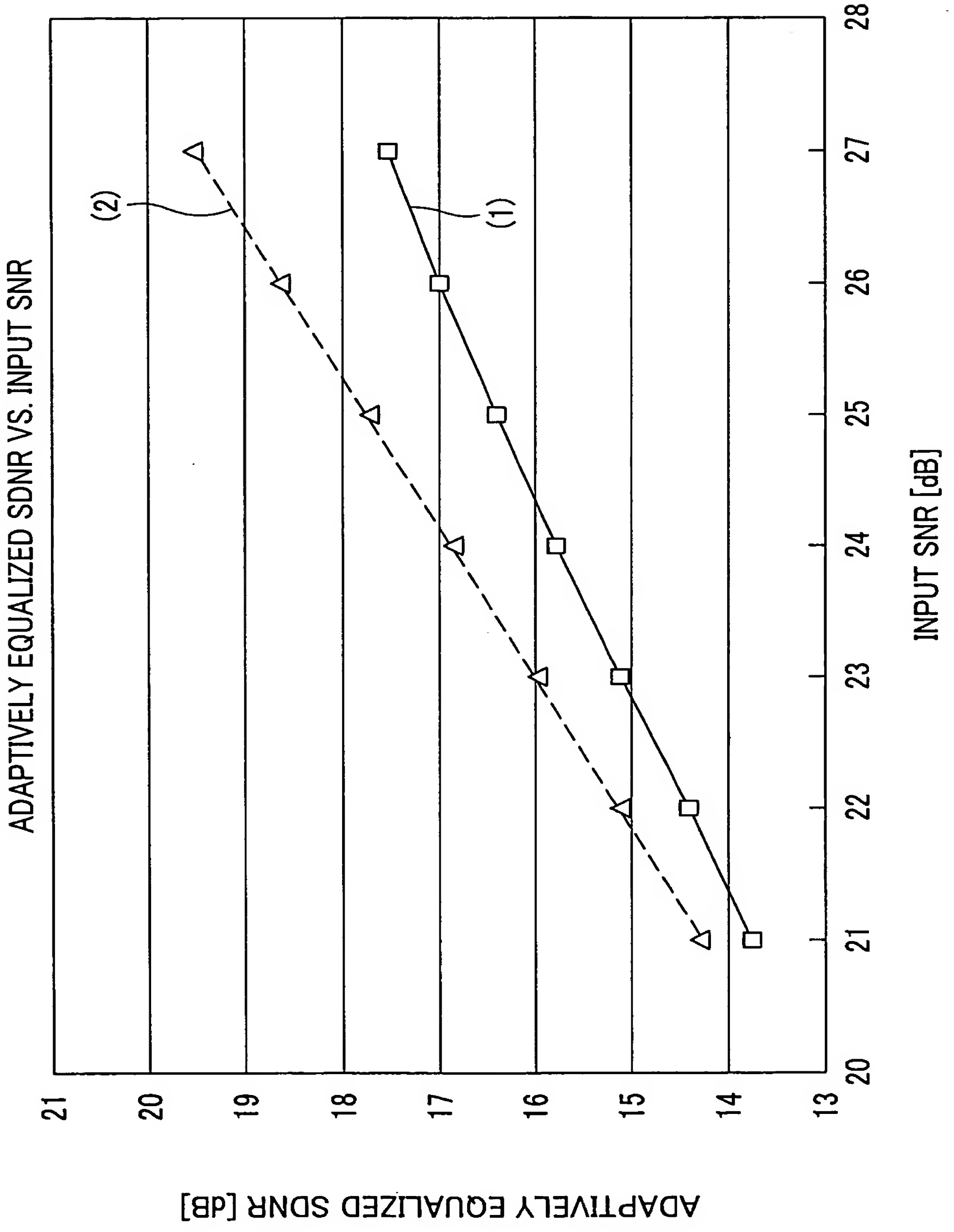

FIG.10

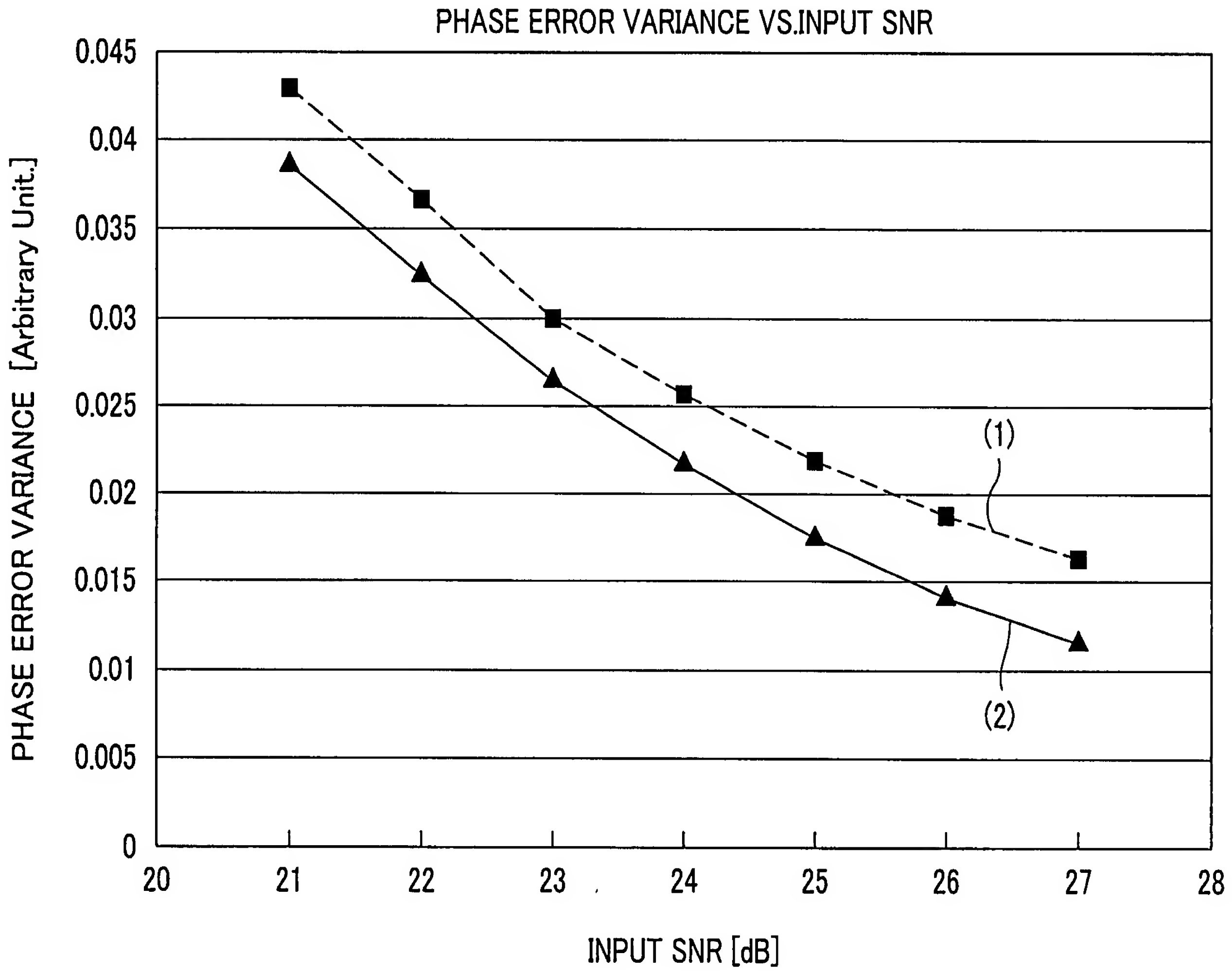
PHASE ERROR VARIANCE VS.INPUT SNR
PHASE ERROR VARIANCE [Arbitrary Unit.]
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
20
21
22
23
24
25
26
27
28
INPUT SNR [dB]
(1)
(2)

FIG.11

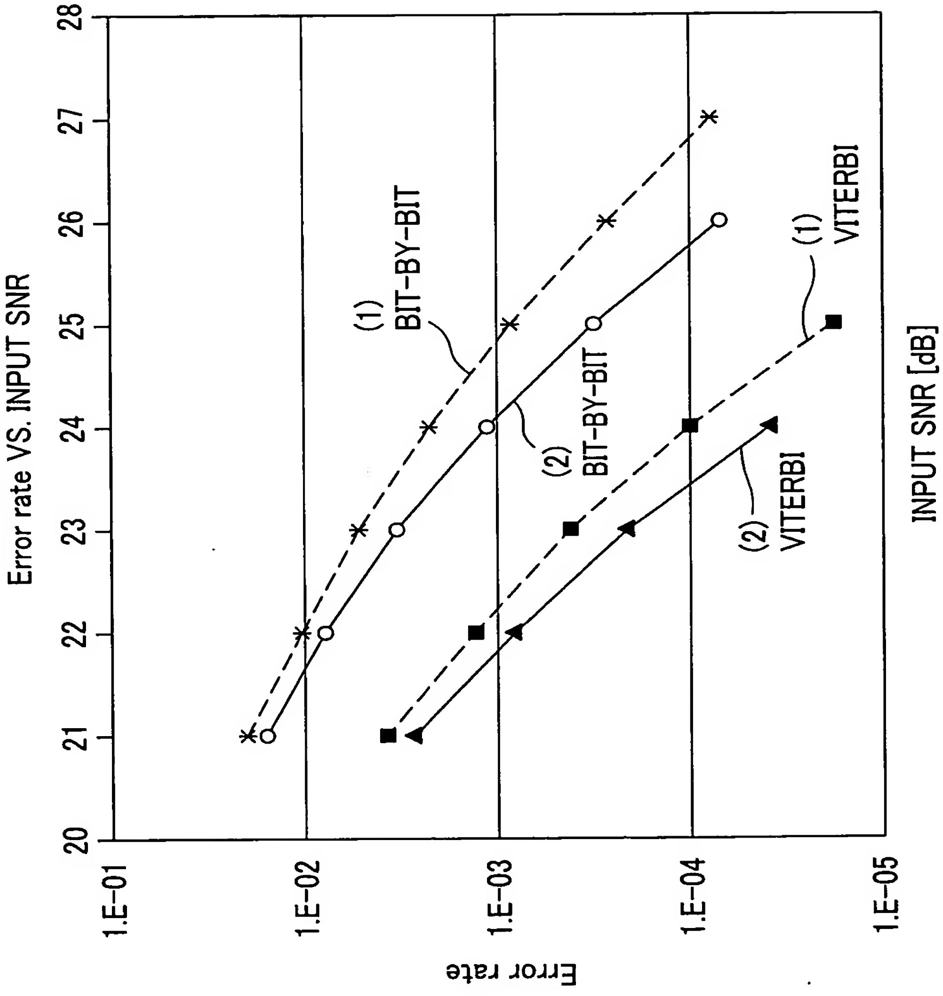
Error rate VS. INPUT SNR
Error rate
INPUT SNR [dB]
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
20
21
22
23
24
25
26
27
28
(1) BIT-BY-BIT
(2) BIT-BY-BIT
(1) VITERBI
(2) VITERBI

FIG.12

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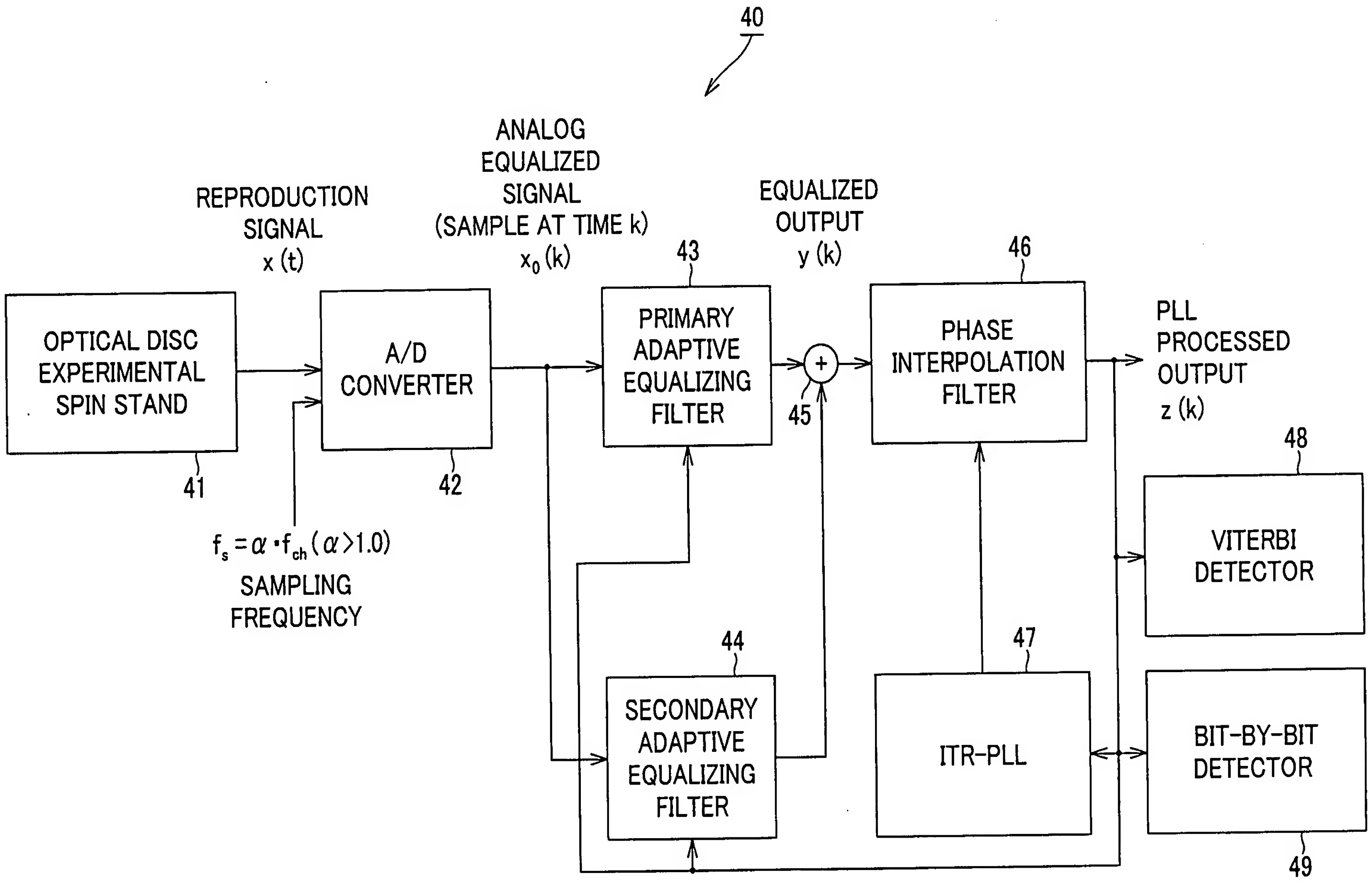

FIG.13

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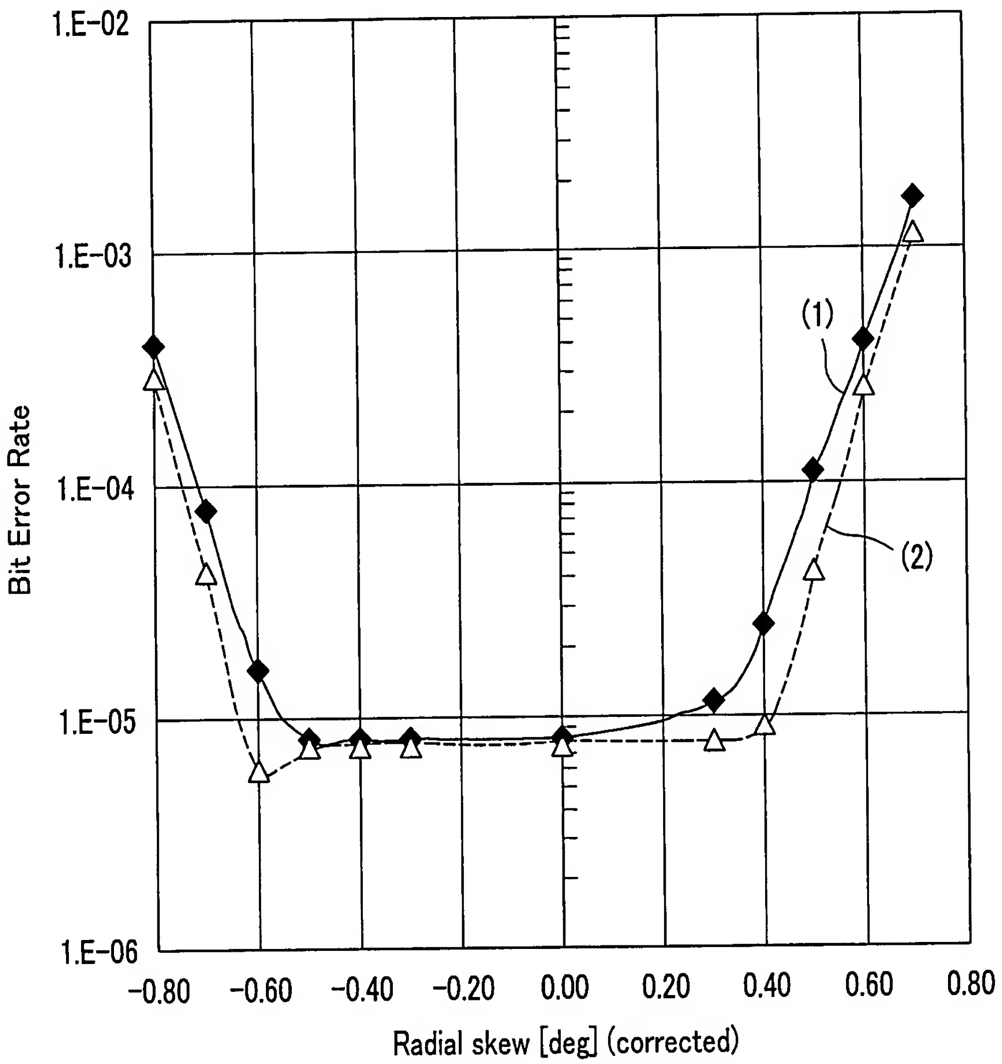

FIG.14